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| S.No | Lect  No | Topic to be discussed | Objective of lecture | Outcome of the Lecture | Book Referred | From page to |
| 1 | 1 | **Number Systems, Basic Logic Gates & Boolean Algebra:** Binary Arithmetic & Radix representation of different numbers. | To introduce basic postulates of Boolean algebra and show the correlation between Boolean expressions. To introduce the methods for simplifying Boolean expressions. | Students will be able to Analyze different methods used for simplification of Boolean expressions. | Text Book 1 |  |
| 2 |  | Sign & magnitude representation, . Fixed point representation | Students will be able to Analyze different methods used for simplification of Boolean expressions. | Text Book 1 |  |
| 3 |  | complement notation, various codes & arithmetic in different codes & their inter conversion | Students will be able to Analyze different methods used for simplification of Boolean expressions. | Text Book 1 |  |
| 4 |  | Features of logic algebra, postulates of Boolean algebra. | Students will be able to Analyze different methods used for simplification of Boolean expressions. | Text Book 1 |  |
| 5 |  | Theorems of Boolean algebra.Boolean function | Students will be able to Analyze different methods used for simplification of Boolean expressions. | Text Book 1 |  |
| 6 |  | Derived logic gates: Exclusive-OR, NAND, NOR gates,their block diagrams and truth tables | Students will be able to Analyze different methods used for simplification of Boolean expressions. | Text Book 1 |  |
| 7 |  | Logic diagrams from Boolean expressions and vica-versa | Students will be able to Analyze different methods used for simplification of Boolean expressions. | Text Book 1 |  |
| 8 |  | . Converting logic diagrams to universal logic. Positive, negative and mixed logic.Logic gate conversion. | Students will be able to Analyze different methods used for simplification of Boolean expressions. | Text Book 1 |  |
| 9 |  | **Digital Logic Gate Characteristics:** TTL logic gate characteristics: Theory &  operation of TTL NAND gate circuitry.. | To outline the procedures for the analysis and design of combinational circuits. | Students will be able to Design and implement Combinational circuits. | Text Book 1 |  |
| 10 |  | Open collector TTL. Three state output  logic. | Students will be able to Design and implement Combinational circuits. | Text Book 1 |  |
| 11 |  | TTL subfamilies.MOS & CMOS logic families. Realization of logic gates in RTL, | Students will be able to Design and implement Combinational circuits. | Text Book 1 |  |
| 12 |  | DTL, ECL, C-MOS & MOSFET. Interfacing logic families to one another | Students will be able to Design and implement Combinational circuits. | Text Book 1 |  |
| 13 |  | TTL subfamilies.MOS & CMOS logic families. | Students will be able to Design and implement Combinational circuits. | Text Book 1 |  |
| 14 |  | Realization of logic gates in RTL,  DTL, ECL, | Students will be able to Design and implement Combinational circuits. | Text Book 1 |  |
| 15 |  | Realization of logic gates in  C-MOS & MOSFET. | Students will be able to Design and implement Combinational circuits. | Text Book 1 |  |
| 16 |  | Interfacing logic families to one another. | Students will be able to Design and implement Combinational circuits. | Text Book 1 |  |
| 17 |  | **Minimization Techniques:** Minterm, Maxterm, | To outline the formal procedures for the analysis and design of sequential circuits. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 18 |  | Karnaugh Map, K map upto 4  variables. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 19 |  | Simplification of logic functions with K-map | Students will be able to Design and implement synchronous and asynchronous sequential ircuits. | Text Book 1 |  |
| 20 |  | Conversion of truth tables in POS and SOP form. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 21 |  | Incomplete specified functions.  Variable mapping. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 22 |  | Quinn-McKlusky minimization techniques |  | Text Book 1 |  |
| 23 |  | **Combinational Systems:** Combinational logic circuit design, | To introduce the concept of memories and programmable logic devices. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 24 |  | Half adders. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 25 |  | full adder,subtractor. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 26 |  | Binary serial and parallel adders. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 27 |  | BCD adder.Binary multiplier. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 28 |  | Decoder: Binary to Graydecoder, BCD to decimal,. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 29 |  | BCD to 7-segment decoder | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 31 |  | Multiplexer, demultiplexer, | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 32 |  | encoder. Octal to binary | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 33 |  | BCD to excess-3 ncoder.Diode  switching matrix. | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 34 |  | Design of logic circuits by multiplexers, | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 35 |  | encoders, decoders and  demultiplexers | Students will be able to Design and implement synchronous and asynchronous sequential circuits. | Text Book 1 |  |
| 36 |  | **Sequential Systems:** Latches, flip-flops | To introduce the concept of synchronous and asynchronous sequential circuits and to design Combinational and Sequential circuits using VERILOG. | Students will be able to Write simple HDL codes for the circuits. | Text Book 1 |  |
| 37 |  | R-S, D- flip flops. | Students will be able to Write simple HDL codes for the circuits. | Text Book 1 |  |
| 38 |  | J-K, Master Slave | Students will be able to Write simple HDL codes for the circuits. | Text Book 1 |  |
| 39 |  | Conversions of flip-flops. | Students will be able to Write simple HDL codes for the circuits. | Text Book 1 |  |
| 40 |  | **Counters:** Synchronous & asynchronous ripple and decade counters | Students will be able to Write simple HDL codes for the circuits. | Text Book 1 |  |
| 41 |  | Modulus counter, skipping state counter | Students will be able to Write simple HDL codes for the circuits. | Text Book 1 |  |
| 42 |  | counter design, state diagrams and state reduction techniques | To introduce the concept of synchronous and asynchronous sequential circuits and to design Combinational and Sequential circuits using VERILOG. | Students will be able to Write simple HDL codes for the circuits. | Text Book 1 |  |
| 43 |  | Ring counter. Counter applications. | Students will be able to Write simple HDL codes for the circuits. | Text Book 1 |  |
| 44 |  | Registers: buffer register, shift  register. | Students will be able to Write simple HDL codes for the circuits. | Text Book 1 |  |